WHAT IS CLAIMED IS:

1. A method of fabricating a semiconductor device, the method comprising:

providing a workpiece;

depositing a porous dielectric material over the workpiece;

forming a pattern in the porous dielectric material, the pattern comprising sidewalls;

depositing a photosensitive material over the porous dielectric material, wherein the photosensitive material forms a barrier region of photosensitive material within the sidewalls of the pattern in the porous dielectric material, over the sidewalls of the pattern in the porous dielectric material, or both within and over the sidewalls of the pattern in the porous dielectric material; and

developing the photosensitive material.

2. The method according to Claim 1, wherein forming the pattern in the porous dielectric material comprises forming a single or dual damascene pattern.

3. The method according to Claim 1, wherein depositing the porous dielectric material comprises depositing a low dielectric constant material.

4. The method according to Claim 3, wherein depositing the low dielectric constant material comprises depositing a material having a dielectric constant of 3.0 or less.

5. The method according to Claim 3, wherein depositing the low dielectric constant material comprises depositing porous methylsilsesquioxane (MSQ), porous inorganic materials, porous CVD materials, porous organic materials, other non-low-k dielectric materials, or combinations thereof.

6. The method according to Claim 1, wherein depositing the photosensitive material comprises spinning on a material compatible with the porous dielectric material.

7. The method according to Claim 6, wherein depositing the porous dielectric material comprises depositing porous methylsilsesquioxane (MSQ), a porous inorganic material, a porous CVD material, a porous organic material, or a non-low-k dielectric material, and depositing the photosensitive material comprises depositing a MSQ material, an inorganic material, a CVD material, an organic material, or a non-low-k dielectric material.

8. The method according to Claim 1, wherein depositing the photosensitive material comprises depositing photosensitive polyimide, a photosensitive organic material, a photosensitive inorganic material, or benzocyclobutane (BCB).

9. The method according to Claim 1, wherein the porous dielectric material comprises a plurality of pores, wherein the barrier region comprises photosensitive material soaked into the sidewalls of the porous dielectric material pattern by about one or two pores.

10. The method according to Claim 1, wherein the barrier region comprises photosensitive material soaked into the sidewalls of the porous dielectric material pattern by about 50 Å or less.

11. The method according to Claim 1, wherein developing the photosensitive material comprises exposing the workpiece to ultraviolet (UV) light.

12. The method according to Claim 11, wherein exposing the workpiece to light comprises exposing the workpiece to DUV light in 365 nm, 248 nm, or 193 nm wavelengths.

13. The method according to Claim 1, further comprising:

depositing a liner over the porous dielectric material and barrier region of photosensitive material; and

depositing a conductive material over the liner to fill the pattern in the porous dielectric material.

14. The method according to Claim 13, wherein depositing the conductive material comprises depositing copper.

15. The method according to Claim 1, wherein all of the photosensitive material is removed from the patterned porous dielectric material after developing the photosensitive material.

16. The method according to Claim 1, further comprising depositing an etch stop layer over the porous dielectric material, before forming the pattern in the porous dielectric material.

17. The method according to Claim 16, wherein the etch stop layer comprises about 100 to 1000 Å of a silicon carbon based material, a carbo-nitride material, a spin-on cap material, silicon nitride, silicon oxides, other insulating materials, a metal, or combinations thereof.

18. A semiconductor device, comprising:

a workpiece;

a porous dielectric material disposed over the workpiece, the porous dielectric material comprising a pattern, the pattern comprising sidewalls; and

a barrier region of photosensitive material disposed within, over, or within and over the porous dielectric material sidewalls.

19. The semiconductor device according to Claim 18, wherein the pattern in the porous dielectric material comprises a single or dual damascene pattern.

20. The semiconductor device according to Claim 18, wherein the porous dielectric material comprises a low dielectric constant material.

21. The semiconductor device according to Claim 18, wherein the low dielectric constant material comprises a dielectric constant of 3.0 or less.

22. The semiconductor device according to Claim 18, wherein the low dielectric constant material comprises porous methylsilsesquioxane (MSQ), porous inorganic materials, porous CVD materials, porous organic materials, other non-low-k dielectric materials, or combinations thereof.

23. The semiconductor device according to Claim 18, wherein the photosensitive material comprises a spin-on material compatible with the porous dielectric material.

24. The semiconductor device according to Claim 23, wherein the porous dielectric material comprises porous methylsilsesquioxane (MSQ), a porous inorganic material, a porous CVD material, a porous organic material, or a non-low-k dielectric material, and the photosensitive material comprises a MSQ material, an inorganic material, a CVD material, an organic material, or a non-low-k dielectric material.

25. The semiconductor device according to Claim 18, wherein the photosensitive material comprises photosensitive polyimide, a photosensitive organic material, a photosensitive inorganic material, or benzocyclobutane (BCB).

26. The semiconductor device according to Claim 18, wherein the porous dielectric material comprises a plurality of pores, wherein the barrier region of photosensitive material is disposed within the sidewalls of the porous dielectric material pattern by about one or two pores.

27. The semiconductor device according to Claim 18, wherein the barrier region of photosensitive material is disposed within the sidewalls of the porous dielectric material pattern by about 50 Å or less.

28. The semiconductor device according to Claim 18, wherein photosensitive material is developable by exposing the workpiece to ultraviolet (UV) light.

29. The semiconductor device according to Claim 28, wherein photosensitive material is developable by exposing the workpiece to DUV light in 365 nm, 248 nm, or 193 nm wavelengths.

30. The semiconductor device according to Claim 18, further comprising:

a liner disposed over the porous dielectric material and the photosensitive material disposed within the sidewalls of the porous dielectric material pattern; and

a conductive material disposed over the liner, filling the porous dielectric material pattern.

31. The semiconductor device according to Claim 30, wherein the conductive material comprises copper.

32. The semiconductor device according to Claim 18, further comprising an etch stop layer disposed over the porous dielectric material.

33. The semiconductor device according to Claim 32, wherein the etch stop layer comprises about 100 to 1000 Å of a silicon carbon based material, a carbo-nitride material, a spin-on cap material, silicon nitride, silicon oxides, other insulating materials, a metal, or combinations thereof.

34. The semiconductor device according to Claim 32, wherein the barrier region comprises photosensitive material disposed over the porous dielectric material sidewalls beneath the etch stop layer, and wherein the barrier region comprise substantially vertical sidewalls.